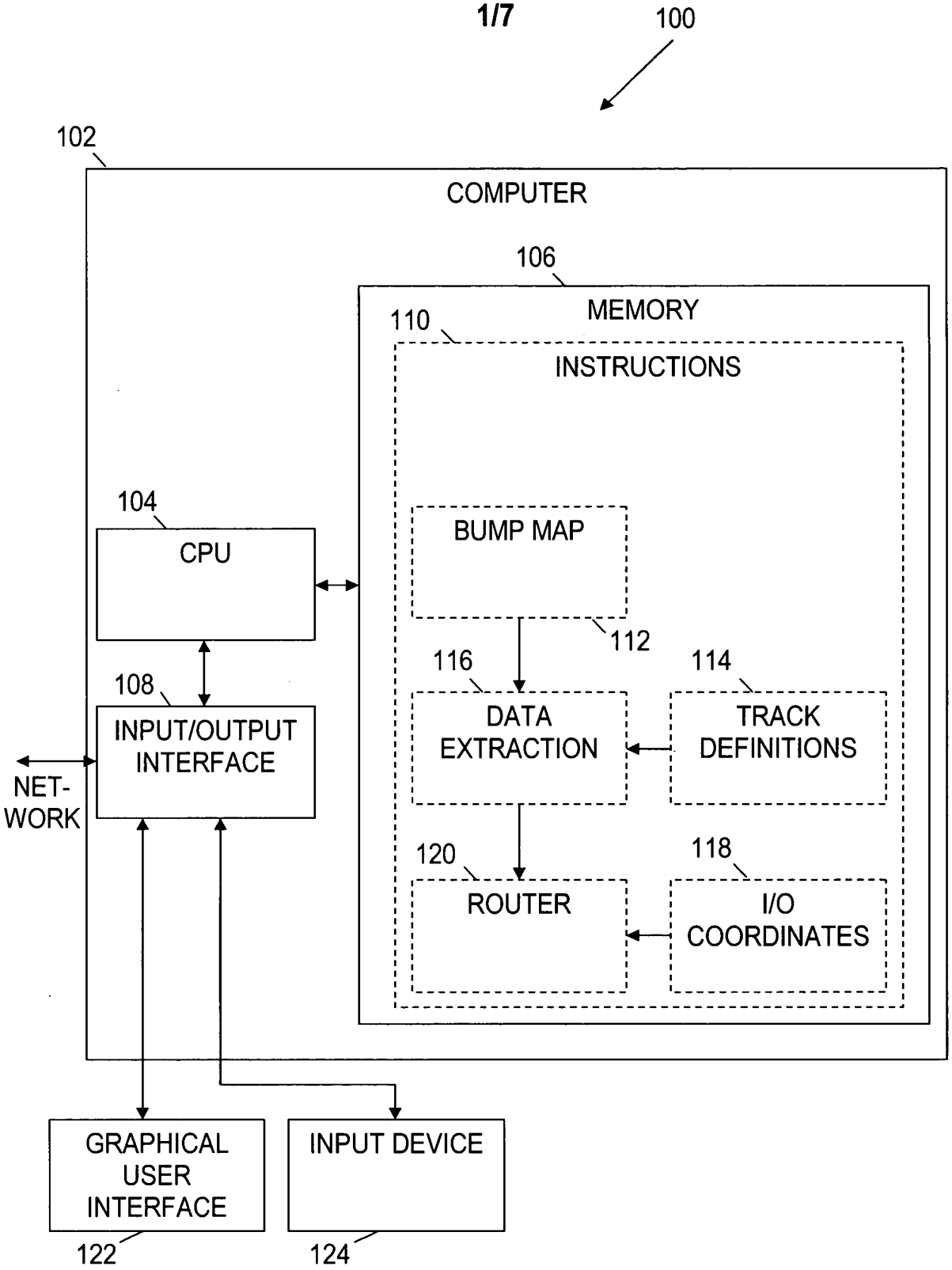
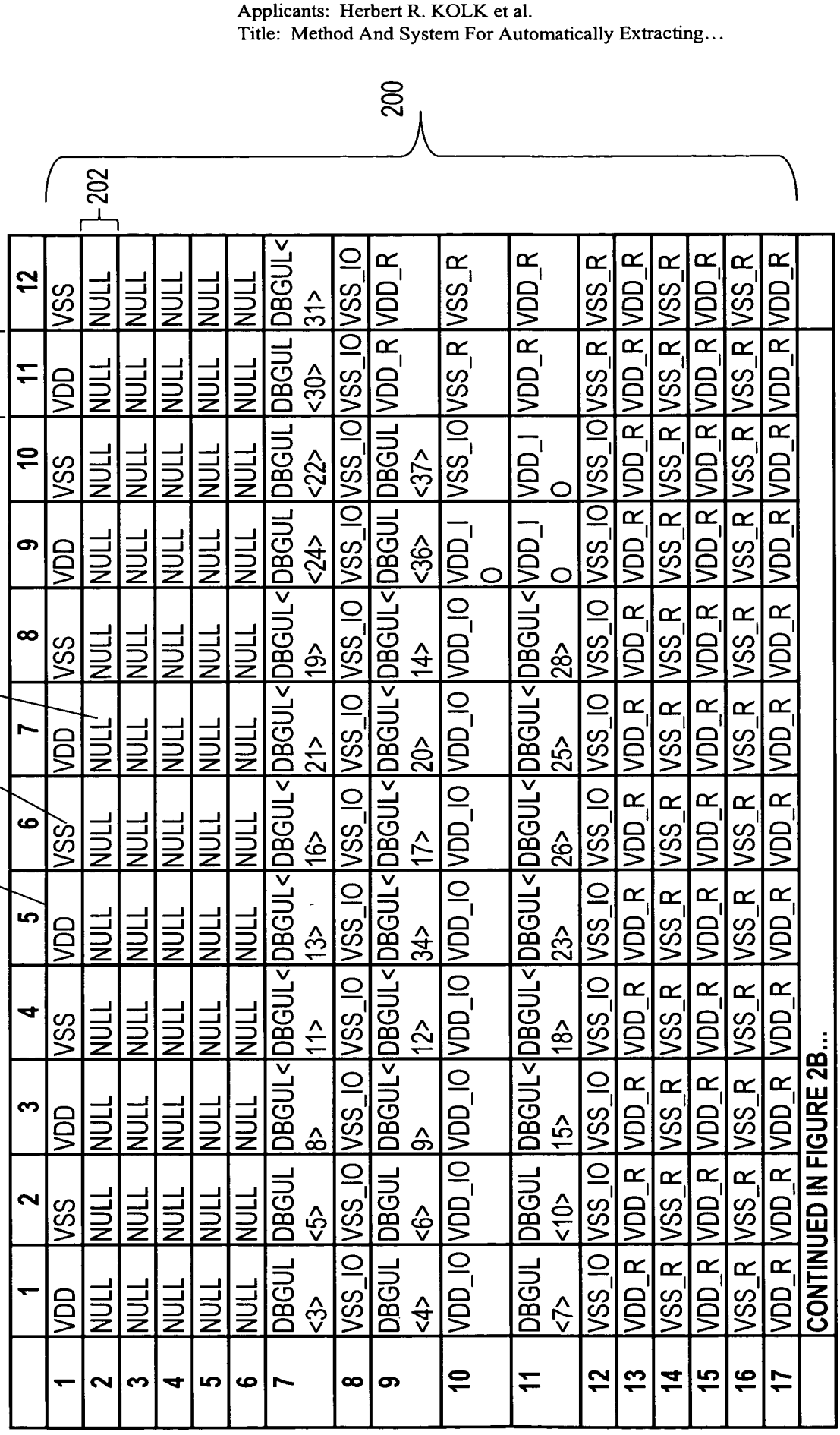

100
102
COMPUTER
106
MEMORY
110
INSTRUCTIONS
104
CPU
BUMP MAP
112
116
DATA EXTRACTION
114
TRACK DEFINITIONS
108
INPUT/OUTPUT INTERFACE
NET-WORK
120
ROUTER
118
I/O COORDINATES
GRAPHICAL USER INTERFACE
122
INPUT DEVICE
124

FIGURE 1



	1	2	3	4	5	6	7	8	9	10	11	12
1	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS
2	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL
3	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL
4	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL
5	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL
6	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL	NULL
7	DBGUL <3>	DBGUL <5>	DBGUL <8>	DBGUL <11>	DBGUL <13>	DBGUL <16>	DBGUL <21>	DBGUL <19>	DBGUL <24>	DBGUL <22>	DBGUL <30>	DBGUL <31>
8	VSS_IO	VSS_IO	VSS_IO	VSS_IO	VSS_IO	VSS_IO	VSS_IO	VSS_IO	VSS_IO	VSS_IO	VSS_IO	VSS_IO
9	DBGUL <4>	DBGUL <6>	DBGUL <9>	DBGUL <12>	DBGUL <34>	DBGUL <17>	DBGUL <20>	DBGUL <14>	DBGUL <36>	DBGUL <37>	VDD_R	VDD_R
10	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VSS_IO	VSS_R	VSS_R
11	DBGUL <7>	DBGUL <10>	DBGUL <15>	DBGUL <18>	DBGUL <23>	DBGUL <26>	DBGUL <25>	DBGUL <28>	VDD_IO	VDD_IO	VDD_R	VDD_R
12	VSS_IO	VSS_IO	VSS_IO	VSS_IO	VSS_IO	VSS_IO	VSS_IO	VSS_IO	VSS_IO	VSS_IO	VSS_R	VSS_R
13	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R
14	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R
15	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R
16	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R
17	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R
	CONTINUED IN FIGURE 2B...											

FIGURE 2A

	...CONTINUED FROM FIGURE 2A											
	1	2	3	4	5	6	7	8	9	10	11	12
18	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R
19	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R
20	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R
21	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R
22	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	N_DATA_OUT_H<8>	N_DATA_OUT_H<9>	VDDX1	N_DATA_OUT_ECC_H<1>	N_DATA_OUT_H<23>	N_DATA_OUT_H<22>
23	VDD_R	VDD_R	VDD_R	VDD_R	VDD_R	VSS_R	VSS_IO	VSS_IO	VSS_IO	VSS_IO	VSS_IO	VSS_IO
24	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	VSS_R	N_DATA_OUT_H<15>	VDDX1	N_DATA_OUT_ECC_H<6>	N_DATA_OUT_ECC_H<4>	N_DATA_OUT_H<14>	VDDX1

200

FIGURE 2B

TBL_M8GRID	2	3	4	5		6
GRID NAME USED TO REFERENCE THIS TABLE	WIDTH (ADU)	SPACE TO LEFT (ADU)	SPACE TO RIGHT (ADU)	M8 GRID EDGE OFFSET (ADU)		COMMENTS
IO_3	100	0	50	**1234**		LEFT EDGE OF THIS TRACK RELATIVE TO 0,0 OF CHIP
VSS_1	100	50	50	**1384**		
LCLK_1	50	50	50	**1534**		
VDD_1	100	50	100	**1634**		
VSS_2	100	100	100	**1834**		
CLOCK	150	100	50	**2034**		
VDD_2	100	50	50	**2234**		
VSS_3	100	50	50	**2384**		
LCLK_2	50	50	50	**2534**		
VDD_3	100	50	50	**2634**		
SPECIAL	100	50	50	**2784**		
IO_1	100	50	50	**2934**		
IO_2	100	50	50	**3084**	**3134**	THIS IS USED IN THE DRIVER_SHIFT SPREAD SHEET
IO	450	50	50	**2934**		SPECIAL CENTER FOR WIDE IO

300

BUMP_OFFSET(ADU)	**1234**
M8GRID_PITCH(ADU)	**2000**
M8GRID_LAYER	**8**

302

FIGURE 3

!(DEFINITION CONTINUES UNTIL END STATEMENT, REGION COORDINATES ARE IGNORED)													
402	404												406
MACRO	VSS_VDD_M8												
!COMMENT	LOWER X	LOWER Y	UPPER X	UPPER Y	LAYER	OFFSET	PITCH	WIDTH	SIG	DATA TYPE	GRID PTR		
	0	0	0	0	8	1384	2000	100	VSS	20	VSS_1		
	0	0	0	0	8	1634	2000	100	VDD	21	VDD_1		
	0	0	0	0	8	1834	2000	100	VSS	20	VSS_2		
	0	0	0	0	8	2234	2000	100	VDD	21	VDD_2		
	0	0	0	0	8	2384	2000	100	VSS	20	VSS_3		
	0	0	0	0	8	2634	2000	100	VDD	21	VDD_3	410	
END	!VSS_VDD_M8												
408													

400

FIGURE 4

LOWER X	LOWER Y	UPPER X	UPPER Y								MACRO NAME
4326	5987	268765	32451	0	0	0	0	0	0	0	VSS_VDD_M8

500

FIGURE 5

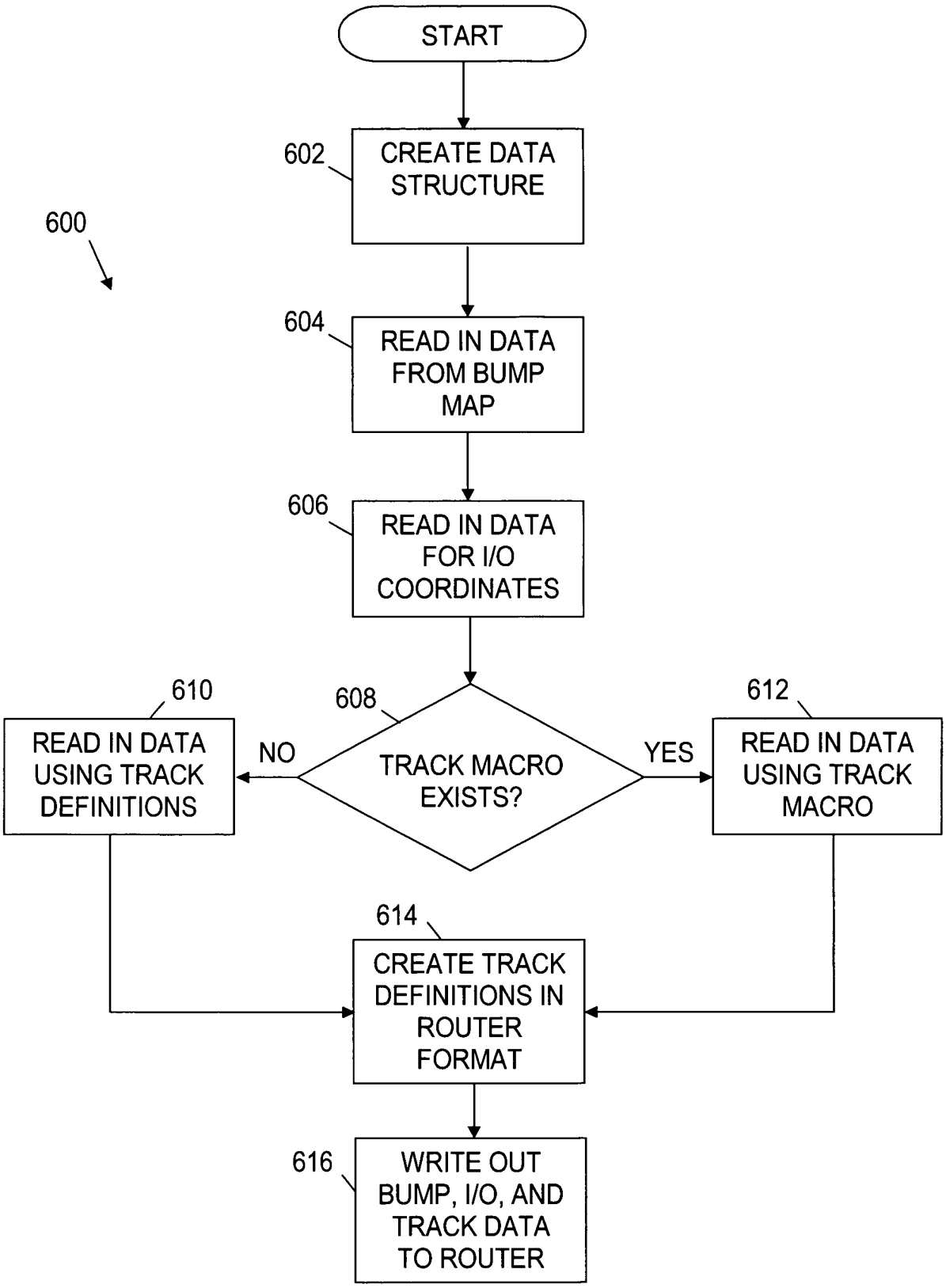

600
START
602
CREATE DATA STRUCTURE
604
READ IN DATA FROM BUMP MAP
606
READ IN DATA FOR I/O COORDINATES
608
TRACK MACRO EXISTS?
NO
YES
610
READ IN DATA USING TRACK DEFINITIONS
612
READ IN DATA USING TRACK MACRO
614
CREATE TRACK DEFINITIONS IN ROUTER FORMAT
616
WRITE OUT BUMP, I/O, AND TRACK DATA TO ROUTER

FIGURE 6

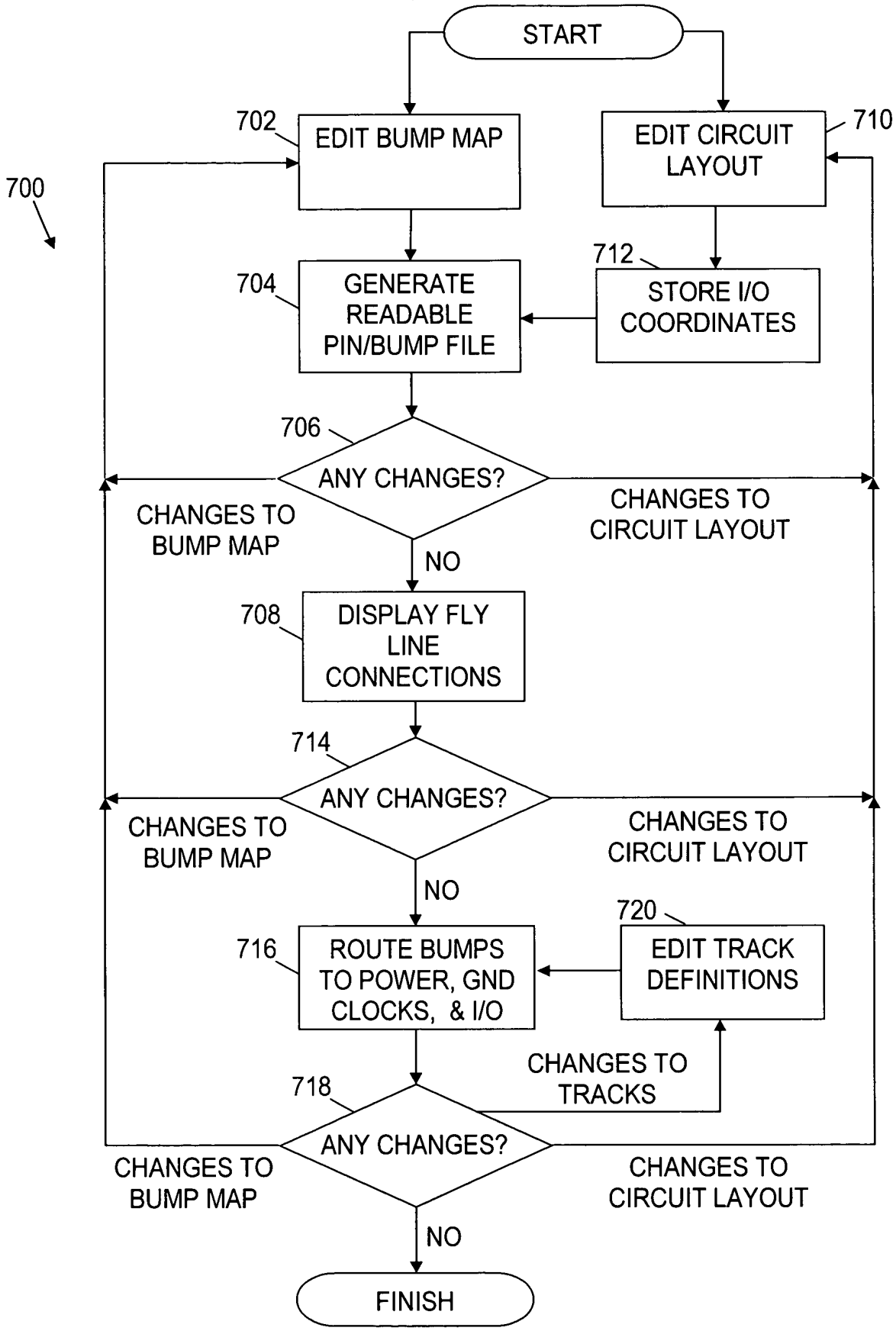

START
700
702
EDIT BUMP MAP
710
EDIT CIRCUIT LAYOUT
712
704
GENERATE READABLE PIN/BUMP FILE
STORE I/O COORDINATES
706
ANY CHANGES?
CHANGES TO BUMP MAP
CHANGES TO CIRCUIT LAYOUT
NO
708
DISPLAY FLY LINE CONNECTIONS
714
ANY CHANGES?
CHANGES TO BUMP MAP
CHANGES TO CIRCUIT LAYOUT
NO
720
716
ROUTE BUMPS TO POWER, GND CLOCKS, & I/O
EDIT TRACK DEFINITIONS
CHANGES TO TRACKS
718
ANY CHANGES?
CHANGES TO BUMP MAP
CHANGES TO CIRCUIT LAYOUT
NO
FINISH

FIGURE 7